AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A recording pulse generator comprising:

a first delay line having plural circuit elements cascaded in multiple stages;

a means that generates plural fine clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof;

a means that selects an arbitrary fine clock form plural fine clocks generated; and

a recording pulse generation means that generates a recording pulse on the basis of a fine clock selected.

2. (original): A recording pulse generator as claimed in Claim 1, further comprising a PLL oscillator that possesses an oscillator with plural circuit elements cascaded in multiple stages, compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage, and controls a voltage of a power supply line according to the phase comparison result, wherein:

the first delay line is connected to the common power supply line with the oscillator, and the circuits elements of the first delay line are equivalent to the circuit elements of the oscillator.

3. (currently amended): A recording pulse generator as claimed in Claim 1 ~~or Claim 2~~, wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

4. (currently amended): A recording pulse generator as claimed in ~~any of~~ Claim 1 ~~through Claim 3~~, wherein the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

5. (currently amended): A recording pulse generator as claimed in ~~any of~~ Claim 1 ~~through Claim 4~~, wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

6. (new): A recording pulse generator as claimed in Claim 2 , wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

7. (new): A recording pulse generator as claimed in Claim 2 , wherein the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

8. (new): A recording pulse generator as claimed in Claim 3 , wherein the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

9. (new): A recording pulse generator as claimed in Claim 6 , wherein the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

10. (new): A recording pulse generator as claimed in Claim 2 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

11. (new): A recording pulse generator as claimed in Claim 3, wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

12. (new): A recording pulse generator as claimed in Claim 4 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

13. (new): A recording pulse generator as claimed in Claim 6 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

14. (new): A recording pulse generator as claimed in Claim 7 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

15. (new): A recording pulse generator as claimed in Claim 8 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

16. (new): A recording pulse generator as claimed in Claim 9 , wherein the recording pulse generation means is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.